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Solution-processed CdS transistors with high electron mobility†

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Solution-processed CdS field effect transistors (FETs) and solar cells are demonstrated *via* spin-coating and thermal annealing of soluble cadmium thiolate compounds. The synthesis is carried out in one simple step using cadmium oxide and tertiary alkane thiols. The cadmium thiolates are soluble in organic solvents such as chloroform and may be spin-coated, like organic semiconductors, to form thin films. The cadmium thiolate films decompose rapidly at 300 °C to yield semiconducting cadmium sulfide films. FETs are easily fabricated using these films and exhibit electron mobilities of up to 61 $cm^2 V^{-1} s^{-1}$, which compare favourably to FETs prepared from other solution-processed materials such as organic semiconductors, inorganic nanoparticles or chalcogenide films. Initial attempts to prepare hybrid bilayer solar cells were successfully realized by spin-coating a p-type semiconducting polymer layer on top of the n-type CdS film. These devices show significant photocurrent response from both the CdS and polymer layers, indicating that the CdS films are able to participate in photo-induced electron transfer from the polymer to the CdS layer as well as photo-induced hole transfer from CdS to the polymer layer.

The rapid development and large demand for consumer electronics ranging from flat-panel televisions to mobile devices has spurred a great interest in routes to achieve high-performance field effect transistors (FETs) using low-cost materials, flexible substrates and novel processing techniques. In this regard, routes to fabricate FETs *via* solution processing techniques have attracted a great deal of academic and commercial interest, as solution-processed devices are amenable to mass-production techniques such as ink-jet printing and roll-to-roll processing; strategies have been developed to process both inorganic[1] and organic semiconductor materials in these ways.[2,3] Solution-processed organic FETs have developed rapidly and show good performance, however, mobilities of conjugated organic materials still lag behind inorganic materials. Graphene based devices[4] as well as solution-processed inorganic nanoparticles (NPs)[5,6] and nanosheets[7] have emerged as routes to easily prepare FETs under mild temperatures and pressures, with excellent results, demonstrating that the investigation of novel processing procedures for FETs can be fruitful.

Cadmium sulfide (CdS) shows great potential as a versatile semiconductor that can be deposited in a number of ways. FETs have been prepared from CdS by thermal evaporation, yielding charge carrier mobilities (μ) of ~50 $cm^2 V^{-1} s^{-1}$,[8] using chemical bath deposition to yield μ in the range of 0.1 to 9 $cm^2 V^{-1} s^{-1}$,[9–14] and up to 350 $cm^2 V^{-1} s^{-1}$ by chemical vapor deposition,[15] however, these methods are expensive and/or laborious compared to methods such as spin-coating, doctor blading, screen printing or ink-jet printing. Encouraging results have been obtained *via* the processing of CdS FETs from CdS or CdS/CdSe core–shell NP solutions, yielding μ of up to 30 $cm^2 V^{-1} s^{-1}$.[13,16,17] However, the operation of FETs does not rely on quantum confinement within nanostructures and carrier transport between NPs may be limited by tunnelling barriers between individual NPs,[18] thus, it is of interest to explore routes to obtain bulk CdS *via* solution processing routes.

The deposition of bulk chalcogenide films directly from solution (*i.e.* spin-coating or doctor blading) is not well known due to the insolubility of chalcogenide semiconductors. Some chalcogenides may be processed using hydrazine, which has remarkable solvating effects on many chalcogenides, however, the toxicity and reactivity of hydrazine leave a need for a more conventional solvent to process chalcogenides. Additionally, films processed with hydrazine must be annealed at 400 °C in order to ensure conversion of the solvated material to the pure chalcogenide, in order to obtain the best semiconducting properties.[19] In one report, CdS FETs were prepared by the thermal decomposition of a molecular precursor, yielding bulk CdS with a μ of up to 48 $cm^2 V^{-1} s^{-1}$,[20] substantiating this route as an effective way to obtain semiconducting CdS films.

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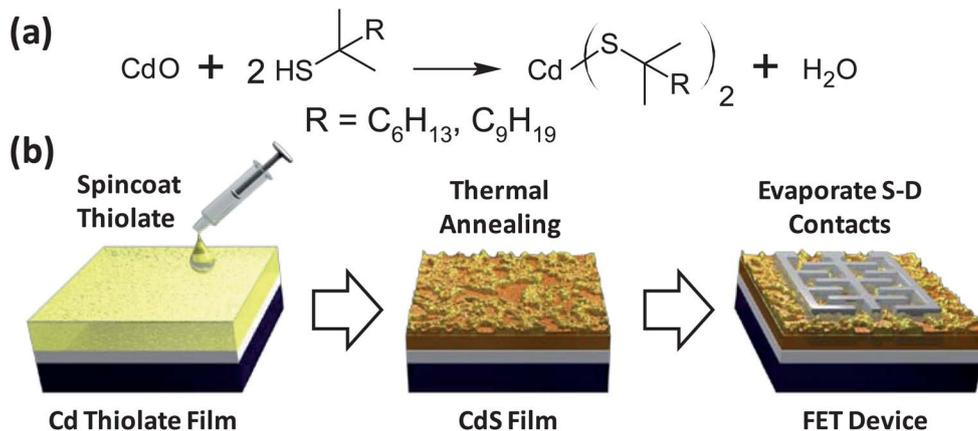
Fig. 1 Schematic diagrams. (a) Synthetic scheme for thiolate preparation and (b) illustration of device processing procedure for preparing FETs from the soluble thiolates.

Here, we report the preparation of high-mobility CdS films suitable for use in FETs *via* spin-coating and thermal annealing of cadmium thiolates. Cadmium thiolates have previously been employed as routes to obtaining CdS *via* photodecomposition or thermal decomposition, yielding suspensions or composites of NPs or nanostructures in various media.[21–25] In one case, solar cells were prepared *via* the thermal decomposition of a Cd thiolate/conjugated polymer mixture, however, little photocurrent generation was observed and current voltage characteristics of the devices were not reported.[26] The preparation of FET devices *via* the thermal decomposition of solution processed cadmium thiolates currently remains unexplored. This approach shows particular promise in the realm of organic–inorganic hybrid devices, as the inorganic film may be deposited using techniques compatible with organic semiconductors while the preparation of the thiolate precursors is exceedingly simple.

The thiolate precursors used in this study are prepared simply from cadmium oxide (or acetate) and long, tertiary alkyl chain thiolates (Fig. 1a). The use of these starting materials ensures the absence of extraneous elements (*i.e.* alkali metals, halides, nitrogen bases) which might later contaminate and interfere with the electronic properties of the CdS end product. The reaction between cadmium oxide and the thiols is simple and economical, however, it requires several weeks to complete while the reaction between cadmium acetate and the thiols proceeds overnight. Tertiary alkyl thiols are chosen as tertiary alkyl cadmium thiolates have previously been shown to decompose cleanly to form CdS upon heating at moderate temperatures in the range of 250 to 300 °C.[27,28] Although short alkyl chain cadmium thiolates are insoluble, the use of tertiary dodecyl and tertiary nonylthiols yields soluble cadmium thiolate precursors. After a mixture of cadmium oxide (or acetate), tertiary alkyl thiol and chloroform have magnetically stirred until the solid has dissolved, the mixture is passed through a 0.45 μm PTFE syringe filter to remove undissolved solids and precipitated into ethanol, washed with ethanol, then dried under a stream of argon. The isolated cadmium thiolate can then be dissolved in chloroform and spin-coated onto substrates just as a conjugated polymer or conjugated small

molecule film might be processed, and subsequently annealed, as illustrated schematically in Fig. 1b, to obtain CdS films.

Thermogravimeteric analysis (TGA) of the cadmium *tert*-nonanethiolate (**CdTNT**) (Fig. 2a) shows that the powdered material rapidly decomposes in the range of 224 to 239 °C to 38.6% of its original mass, ultimately reaching 37.6% of its original mass by 400 °C, while cadmium *tert*-dodecanethiolate (**CdTDT**) (Fig. 2b) decomposes in the range of 224 to 241 °C to 30.5% of its original mass, ultimately reaching 29.5% of its original mass by 400 °C, consistent with the conversion of the thiolate to CdS and consistent with the reported decomposition of other cadmium thiolates.[14] Although TGA indicates that **CdTNT** and **CdTDT** powders decompose to CdS at temperatures near 240 °C, a hotplate setting of 300 °C was used to consistently decompose spin-coated films of **CdTNT** and **CdTDT** and yield CdS films on silicon or glass substrates. A hotplate setting of 250 °C was not adequate to reliably decompose the film, likely
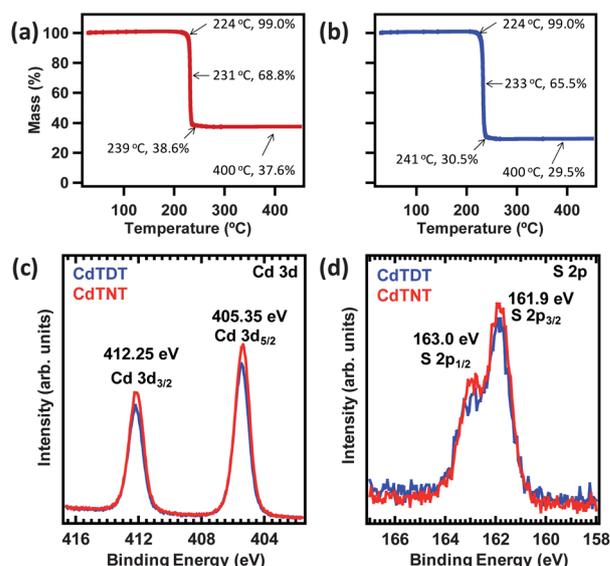

Fig. 2 Characterization. TGA plots of (a) **CdTNT** and (b) **CdTDT**. X-ray photoelectron (c) Cd 3d and (d) S 2p spectra of CdS films.

because the top surface of the film is in contact with an ambient nitrogen atmosphere may be at a marginally lower temperature than the temperature measured by the hotplate.

X-ray photoelectron spectroscopy (XPS) spectra of CdS films prepared from **CdTNT** and **CdTDT** on Si/Au substrates are consistent with the presence of CdS (Fig. 2c). Detailed XPS plots of the Au, Cd and S signals can be found in the ESI.†

UV-vis spectra of films prepared on glass substrates (ESI†) show absorption spectra having an onset of 524 nm and an optical bandgap of 2.37 eV, close to the reported optical bandgap (2.38 eV) for thermally evaporated bulk CdS films using a substrate temperature of 300 °C.[29] Ultraviolet photoelectron spectra (ESI†) indicate a work function of 4.81 eV, a valence band energy of 6.65 eV and a conduction band energy of 4.28 eV. X-ray diffractograms were collected for films prepared on Si substrates. Although the intensity of the spectra are low due to the films being very thin, the diffraction peaks fit the pattern expected for the Greenokite phase (ESI†), while Debye–Sherrer analysis of the (110) peak indicate a crystal grain size of approximately 7.0 nm.

Atomic force microscope (AFM) images of the films before and after annealing are shown in Fig. 3. The films of **CdTNT** and **CdTDT** are relatively smooth with root–mean–square (RMS) roughness values of 1.1 and 0.6 nm, respectively. After annealing the thiolate films at 300 °C, the films become much rougher (RMS roughness of 21.7 and 14.4 nm for CdS prepared from **CdTNT** and **CdTDT**, respectively). The average thickness of CdS features is 39 nm for **CdTNT** and 28 nm for **CdTDT**. Multiple layers may be deposited by repeating the spin-coating and

annealing steps in order to obtain thicker films. The films are rough compared to typical organic semiconductors, however, the roughness is comparable to that of CdS films prepared by chemical bath deposition (9 to 13 nm),[30] which are commonly used as window layers in chalcogenide solar cells. The roughness does not adversely affect their FET behavior (discussed later). Nonetheless, we observed that smoother CdS films could be prepared by exposing the spincoated thiolate film to sulfur vapor at a considerably lower temperature (160 °C) by annealing in a 10 cm Petri dish containing a small amount of elemental sulphur powder (50 mg).

FETs were fabricated by depositing CdS films as described above onto silicon substrates with a 200 nm oxide layer, followed by thermal evaporation of Ag source and drain contacts. Immediately after fabrication, transfer curves exhibit n-type behavior with large leakage currents (ESI†). The device characteristics change dramatically after exposure to air for 1 hour. The off-current is reduced dramatically after air exposure; however, the overall current through the device also drops by several orders of magnitude and significant hysteresis is apparent. This increase in resistivity is consistent with effects of oxygen adsorption on thin CdS films previously observed by Bube, *et al.*[31] and the observed depletion of electron density in CdS nanobelt devices upon exposure to oxygen.[32] These undesirable effects can be resolved by one final annealing step at 300 °C in a nitrogen atmosphere, leading to devices with reduced leakage currents and generally good performance. Output and transfer curves of these devices are shown in Fig. 4. **CdTNT** leads to slightly higher μ than **CdTDT**, where μ (average
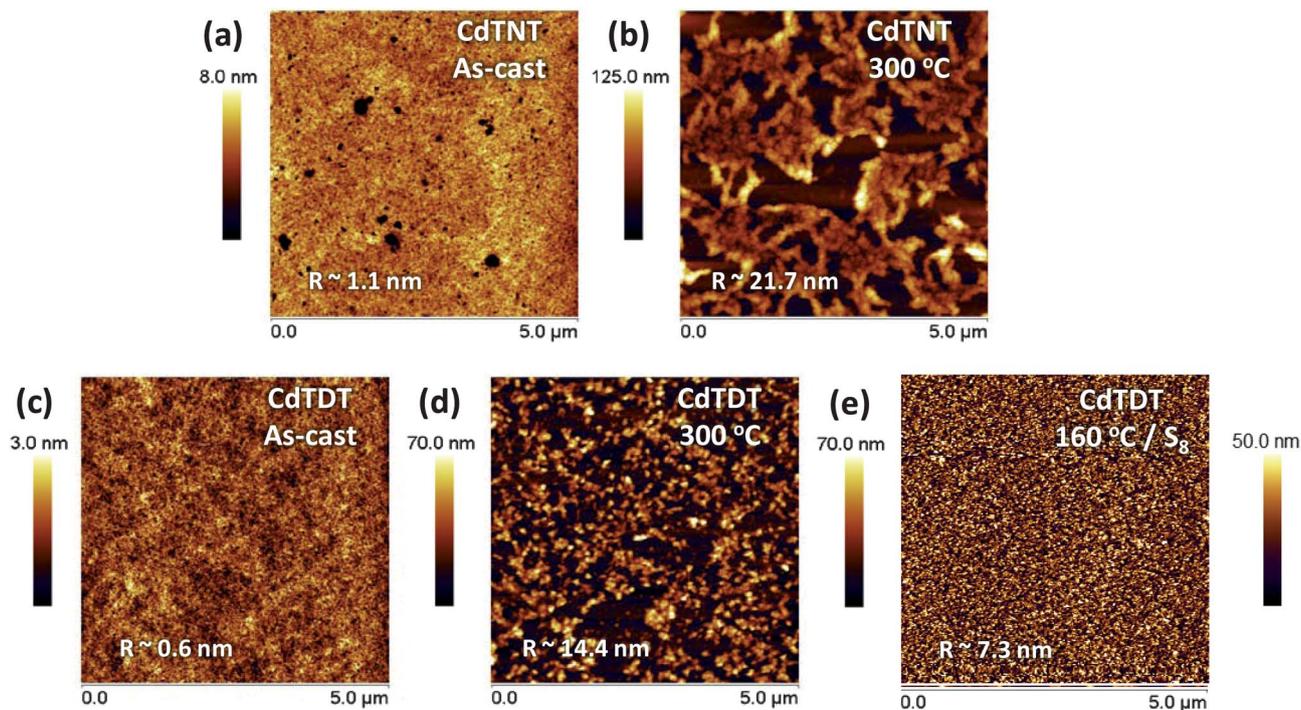

Fig. 3 AFM images. (a) Pristine **CdTNT** film spin-coated from chloroform (8 mg mL^{-1} at 1500 rpm). (b) CdS film after annealing **CdTNT** at 300 °C for 30 min. (c) Pristine **CdTDT** film spin-coated from chloroform (15 mg mL^{-1} at 1500 rpm). (d) CdS film after annealing **CdTDT** at 300 °C for 30 min. (e) CdS film after annealing **CdTDT** at 160 °C for 15 min in the presence of elemental sulfur.

of 8 devices) and on/off ratios are 41 ± 16 cm^2 V^{-1} s^{-1} and >10^5 and 21 ± 9 cm^2 V^{-1} s^{-1} and ~10^6 for devices prepared from **CdTNT** and **CdTDT**, respectively. The highest mobilities observed were 61 and 36 cm^2 V^{-1} s^{-1} for **CdTNT** and **CdTDT**, respectively. The larger, interconnected domains observed in the morphology of CdS films prepared from **CdTNT** seem to result in greater overall mobility. Although AFM images and high-resolution XPS spectra (ESI†) indicate that the films may not completely cover the substrate surface, attempts to increase surface coverage by depositing multiple layers of CdS did not lead to a significant increase in mobility if the precursor solution was at least 8 mg mL^{-1} in the case of **CdTNT** and 15 mg mL^{-1} in the case of **CdTDT**.

Films prepared using lower concentrations lead to poor coverage and lower mobilities which can be improved with multiple coats, however, casting multiple coats has the undesirable affect of increasing the leakage current, leading to lower on/off ratios. Thus, we find that single layers are preferable to multiple layers for FET fabrication. Interestingly, FETs prepared from the smoother CdS films using **CdTDT** annealed at 160 °C in the presence of sulfur show weakly p-type behavior (ESI†).

Due to the air-sensitivity of the films, we briefly evaluated the performance of devices after aging for one week in air or nitrogen. The devices kept in a nitrogen atmosphere (<20 ppm O$_2$) decreased to ~60% of their original μ after one week, but recovered their original characteristics and exhibited a slight improvement in mobility (114% of original μ) after an additional annealing step at 300 °C for 20 minutes in nitrogen. CdS films kept in air for one week prior to electrode evaporation were found to yield typical characteristics including μ of

35 cm^2 V^{-1} s^{-1}, while finished FETs aged in air for 1 week, followed by an annealing step at 300 °C in nitrogen, exhibited similar characteristics before and after aging (91% of original μ). Details of the aging experiments can be found in the ESI.†

In order to evaluate the applicability of the CdS films to other device types, hybrid solar cells were prepared using the CdS films as electron accepting layers in combination with the conjugated polymer poly[[4,8-bis[(2-ethylhexyl)oxy]benzo[1,2-b:4,5-b′]dithiophene-2,6-diyl][3-fluoro-2-[(2-ethylhexyl)carbonyl]thieno[3,4]thiophenediyl]] (PTB7).[33] Devices were prepared using the architecture ITO/CdS/PTB7/MoO$_3$/Au and compared to devices without any CdS layer (ITO/PTB7/MoO$_3$/Au) as well as devices with a ZnO layer[34] (ITO/ZnO/CdS/PTB7/MoO$_3$/Au). Current density–voltage (J–V) characteristics are reported in Fig. 4e while the external quantum efficiency (EQE) of the ITO/ZnO/CdS/PTB7/MoO$_3$/Au device is reported in Fig. 4f, along with the absorption spectra of the CdS and PTB7 layers. The short-circuit current (J$_{SC}$) in the device is found to increase dramatically from 0.12 to 0.92 mA cm^{-2} upon insertion of the CdS layer while the open circuit voltage (V$_{OC}$) increases from 0.014 V to 0.228 V. The V$_{OC}$ of the device can be further improved to 0.350 V by incorporating a ZnO layer between the ITO and CdS layers, yielding a device which produces a J$_{SC}$ of 1.07 mA cm^{-2}, a fill factor of 49% and a power conversion efficiency of 0.2%. The device including a ZnO layer without CdS was found to produce very little photocurrent (J$_{SC}$ ~ 0.01 mA cm^{-2}). The EQE produced by the ITO/ZnO/CdS/PTB7/MoO$_3$/Au architecture shows significant photocurrent from both the CdS layer (which absorbs strongly in the 300 to 500 nm region) and the PTB7 layer (which absorbs strongly in the 550 to 700 nm region),
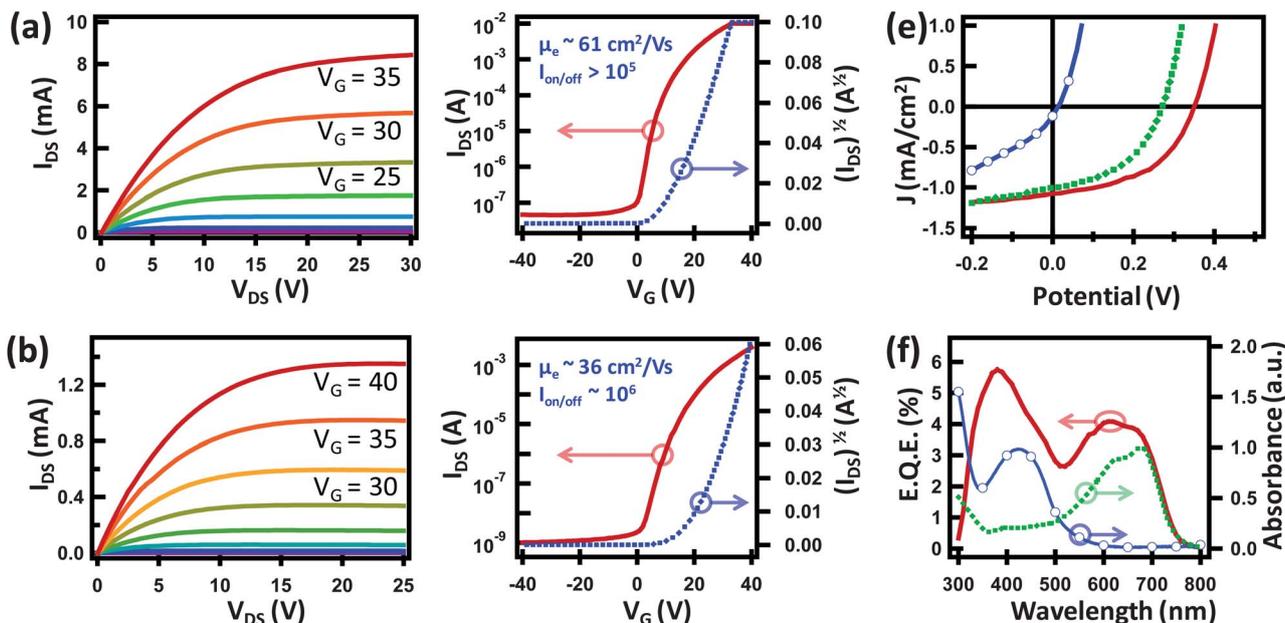

Fig. 4 FET and solar cell device characteristics. (a) and (b) Output curves for CdS devices prepared from **CdTNT** and **CdTDT**, respectively. (c) and (d) Transfer curves for CdS devices prepared from **CdTNT** and **CdTDT**, respectively. (e) J–V characteristics of ITO/PTB7/MoO$_3$/Au (blue trace with circles) ITO/CdS/PTB7/MoO$_3$/Au (dotted green trace) and ITO/ZnO/CdS/PTB7/MoO$_3$/Au (red trace) devices. (f) External quantum efficiency of ITO/ZnO/CdS/PTB7/MoO$_3$/Au device (red trace) compared to the absorption spectra of the CdS film (dotted green trace) and PTB7(blue trace with circles).

demonstrating the ability of the CdS to function as both an electron accepting and hole donating material.

Conclusions

In conclusion, we demonstrate a convenient route to obtain CdS films having good electron mobilities by spin-coating and thermally annealing cadmium thiolate molecules. Although the annealing temperature is somewhat higher than typical for organic semiconductors, the processing procedure is otherwise quite similar to procedures used to prepare organic FETs. The synthetic procedure, however, is considerably simpler than procedures used for typical organic semiconductors (such as Suzuki or Stille couplings) and does not involve the intermediary synthesis of nanoparticles; the thiolate is prepared by simply stirring CdO with an alkyl thiol and can be subsequently processed like an organic semiconductor. We envision that CdS films prepared in this way may be applicable to a wider range of semiconducting devices, including hybrid organic/inorganic devices. Future work will explore the applicability of this technique to other chalcogenide semiconductors and the identification of thiolates which decompose at lower temperatures.

Acknowledgements

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